

Appl. No. 09/783,515  
Amdt. Dated March 15, 2004  
Reply to Office Action of December 15, 2003

CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 (currently amended): A method for supplying a clock signal to processor-controlled apparatuses, which comprises:

~~basing a clock frequency fed to a device for determining a clock time and a clock frequency fed to a processor device at times of no processor load or low processor load, on a quartz frequency of the same quartz, and clocking the processor device with a system clock in third times~~

providing a clock frequency based on a quartz frequency of a clock quartz to a device for determining a clock time; and

providing the clock frequency to a processor device during operational time periods of low processor load or no processor load and otherwise providing a different clock frequency to the processor device.

2 (currently amended): The method according to claim 1, which further comprises:

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~~feeding a first clock frequency based on a first quartz frequency or a frequency derived therefrom, to the device for determining a clock time; selecting the clock frequency to be fed to the processor device as a function of the processor load; and feeding the clock frequency based on the first quartz frequency or on a frequency derived therefrom, to the processor device in first times of no processor load or low processor load~~

selecting a clock signal as a function of processor load such that during operating periods with little or no processor load the same clock signal is provided to a processor device as to the device for determining a clock time; and

during operational time periods with processor loading, providing a clock signal based on a system clock to the processor device.

3 (original): The method according to claim 1, which further comprises generating the quartz frequency with a clock quartz.

4 (currently amended): The method according to claim 1, which further comprises switching the processor device to a

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~~clockless state in second times of during operational time~~  
~~periods with no processor load.~~

*AB*  
5 (currently amended): The method according to claim 2 †, which further comprises clocking the processor device with a reduced frequency ~~in fourth times of during operational time~~  
~~periods with low processor load~~, the reduced frequency being lower than the frequency of the system clock and higher than the quartz frequency or the frequency derived therefrom.

6 (original): The method according to claim 1, which further comprises initiating, with the processor device, a selection of a clock frequency to be fed to the processor device, being lower than a current frequency fed to the processor device.

7 (original): The method according to claim 1, which further comprises initiating, with the processor device, a selection of a clock frequency to be fed to the processor device, being higher than a current clock frequency fed to the processor device.

8 (original): The method according to claim 1, which further comprises initiating, with external events, a selection of a clock frequency to be fed to the processor device, being

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higher than a current clock frequency fed to the processor device.

A3  
9 (original): The method according to claim 1, which further comprises initiating, after expiration of a predefined time period, a selection of a clock frequency to be fed to the processor device, being higher than a current clock frequency fed to the processor device.

10 (original): The method according to claim 1, which further comprises temporarily switching off not-required components of an apparatus as a function of the clock frequency fed to the processor device.

11 (currently amended): In a configuration for supplying a clock signal to processor-controlled apparatuses having a processor device and associated with a device for determining a clock time, the improvement comprising:

a clock selector unit connected to the processor device for selecting a frequency to be fed to the processor device, as a function of a processor load;

an oscillator having a clock quartz for generating a quartz frequency, the oscillator being configured to feed and for

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feeding a clock frequency based on the quartz frequency or a frequency derived therefrom to the device for determining the clock time;

*A3*  
said clock selector unit feeding a clock frequency based on the quartz frequency or on a frequency derived therefrom to the processor device ~~in first times of~~ when there is no processor load or when there is low processor load; and

otherwise the processor device being clocked with a system clock ~~in third times~~.

12 (new): A method for conserving power of a processor device of a processor-controlled apparatus operating by a clock supply system driven according to a usage factor, the method which comprises the steps of:

generating a quartz frequency as a function of a quartz clock;

providing the quartz frequency to a real-time clock;

selecting a clock frequency as a function of processor load;

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generating a clock signal based on the selected clock frequency; and

providing the generated clock signal to the processor device.

13 (new) The method according to claim 12, wherein the clock frequency is selected from the group consisting of a quartz clock frequency, a real-time clock frequency, a standby clock frequency, and a system clock frequency.

14 (new) : The method according to claim 12, wherein the step of selecting a clock frequency as a function of processor load, selects the same quartz frequency as provided to the real-time clock when there is no processor load.

15 (new) : The method according to claim 12, wherein the step of selecting a clock frequency as a function of processor load, selects the same quartz frequency as provided to the real-time clock when there is low processor load.

16 (new) : The method according to claim 12, wherein the step of selecting a clock frequency as a function of processor load is based in part on received processor control signals, interrupt control signals, and timer control signals.